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EXAMINER	
LY, ANH VU H	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,579	SCHMIDT, DOMINIK J.	
	Examiner	Art Unit	
	Anh-Vu H. Ly	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,16-19 and 21-24* is/are rejected.

7)☐ Claim(s) *2,5,20 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *June 16, 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to applicant's amendment filed June 16, 2006. Claims 1-11 and 16-24 are pending.

Specification

2. The disclosure is objected to because of the following informalities: there are numerous missing periods at the end of either sentences and/or paragraphs, e.g., page 1, line 17; page 2, lines 3 and 16; page 3, line 7; etc...

Appropriate correction is required.

Claim Objections

3. Claims 2, 5, and 23 are objected to because of the following informalities:

With respect to claim 2, in line 2, replace "includes" with --include--.

With respect to claims 5 and 23, in line 3, "the one or more general-purpose processor cores" lacks antecedent basis.

Appropriate correction is required.

Information Disclosure Statement

4. The information disclosure statement filed June 16, 2006 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; **each non-patent literature publication** or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 8, in lines 2-3, "a router coupled to route packets to a cellular radio core and a short-range wireless transceiver core of the analog portion" is unclear. It is unclear what element the router coupled to for routing packets to a cellular radio core and a short-range wireless transceiver core of the analog portion.

With respect to claim 10, in lines 2-4, "through a primary and a second communication channel via a first wireless transmission medium and a second wireless transmission medium" is unclear. The communication channel is the transmission medium therefore it is unclear what being claimed.

Claim 9 is automatically rejected as it depends upon rejected dependent claim 8.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for

purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 6, 8, 11, 16, 18-19, and 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanian et al (US Pub 2002/0031166 A1). Hereinafter, referred to as Subramanian.

With respect to claim 1, Subramanian discloses a multi-mode wireless device on a single substrate (Fig. 1A), comprising:

an analog portion integrated on the substrate (Fig. 1B, interface conversion/sector combining 116), including:

a radio frequency front-end (pages 4-5, 47th paragraph, the interface conversion block 116 includes components such as **a radio frequency transceiver** and an analog to digital, A/D, converter coupled to each other in series) to receive an RF signal from an antenna (Fig. 1B, antenna 120); and

an analog to digital converter (ADC) coupled to the RF front-end to digitize the RF signal (pages 4-5, 47th paragraph, the interface conversion block 116 includes components such as a radio frequency transceiver and **an analog to digital, A/D, converter coupled to each other in series**); and

a digital portion integrated on the substrate (Fig. 1B, processors, 102a, 120b, 104, 112, memory 106 and 118, controller 110a), including:

a reconfigurable logic core coupled to receive the digitized RF signal from the ADC (Fig. 1B, DSP/uP 112 coupled to and received data from element 116), the reconfigurable logic core to handle a plurality of wireless communication protocols (page 3, 39th paragraph, the signal

processing functions 16, including the DSP/uP 112, shown have a configurable architecture that enables the device to operate using a wide variety of communication protocols, including CDMA, 3GPP, TDMA, as well as anticipated future protocols);

a plurality of general-purpose processor cores coupled to the reconfigurable logic core (Fig. 1B, processors, 102a, 102b, 104); and

a memory array coupled to the reconfigurable logic core (Fig. 1B, memory 106 and 118 coupled to processor 112 via bus 126 and 130a).

With respect to claim 2, Subramanian discloses that wherein the plurality of wireless communication protocols includes **one** or more of a GSM protocol, GPRS protocol, EDGE protocol and further includes a short-range wireless protocol (page 3, 39th paragraph, the signal processing functions 16, including the DSP/uP 112, shown have a configurable architecture that enables the device to operate using a wide variety of communication protocols, including CDMA, 3GPP, TDMA, as well as anticipated future protocols. Herein, GSM protocol employing TDMA).

With respect to claims 3 and 23, Subramanian discloses that wherein the reconfigurable logic core is to deliver data in parallel to the plurality of general-purpose processor cores (page 19, 188th – 189th paragraphs and Fig. 5, data is delivered parallel to multiple processors by the Function A 504 or the processor 112. Herein, Function A 504 includes multiple sub functions that can be performed in series or parallel).

With respect to claim 4, Subramanian discloses that wherein the reconfigurable logic core is to deliver data in series to the plurality of general-purpose processor cores (page 19, 188th – 189th paragraphs and Fig. 5, data is delivered in series to multiple processors by the Function A 504 or the processor 112. Herein, Function A 504 includes multiple sub functions that can be performed in series or parallel).

With respect to claim 6, Subramanian discloses that wherein at least one of the plurality of general-purpose processor cores includes a multiply-accumulate (MAC) unit (Fig. 2B, a multiple-accumulate (MAC) block 236).

With respect to claim 8, as best understood, Subramanian discloses a router coupled to route packets to a cellular radio core and a short-range wireless transceiver core of the analog portion (Fig. 1B, configurable modem processor 102a routes data packets to interface conversion/sector combining 116).

With respect to claim 11, Subramanian discloses a portable computer system (Fig. 1B), comprising:

a processor (Fig. 1B, controller 114);

a multi-mode wireless device on a single substrate coupled to the processor (Fig. 1B), the device comprising:

an analog portion integrated on the substrate (Fig. 1B, interface conversion/sector combining 116), including:

a cellular radio core having an analog to digital converter (ADC) configured to receive a radio signal from an antenna (pages 4-5, 47th paragraph and Fig. 1, the interface conversion block 116 includes components such as a radio frequency transceiver and **an analog to digital, A/D, converter coupled to each other in series** and coupled to antenna 120), and

a short-range wireless transceiver core (pages 4-5, 47th paragraph, the interface conversion block 116 includes components such as **a radio frequency transceiver** and an analog to digital, A/D, converter coupled to each other in series) to receive an RF signal from an antenna (Fig. 1B, antenna 120); and

a digital portion integrated on the substrate (Fig. 1B, processors, 102a, 120b, 104, 112, memory 106 and 118, controller 110a), including:

a reconfigurable logic core coupled to receive converted data from the ADC (Fig. 1B, DSP/uP 112 coupled to and received data from element 116), the reconfigurable logic core configured to handle a plurality of wireless communication protocols (page 3, 39th paragraph, the signal processing functions 16, including the DSP/uP 112, shown have a configurable architecture that enables the device to operate using a wide variety of communication protocols, including CDMA, 3GPP, TDMA, as well as anticipated future protocols);

a plurality of general-purpose processor cores coupled to the reconfigurable logic core (Fig. 1B, processors, 102a, 102b, 104); and

a memory array coupled to the reconfigurable logic core (Fig. 1B, memory 106 and 118 coupled to processor 112 via bus 126 and 130a).

With respect to claim 16, Subramanian discloses that wherein the reconfigurable logic core includes one or more DSPs (Fig. 1B, DSP/uP 112).

With respect to claim 18, Subramanian discloses that the wireless device further comprising a router coupled to the reconfigurable logic core, cellular radio core, and short-range wireless transceiver core (Fig. 1B, element 102a coupled to DSP 112 and element 116).

With respect to claim 19, Subramanian discloses that wherein the router is to de-correlate data (Fig. 2A, allocator 219 splitting data to multiple kernel planes 201a-i).

With respect to claim 21, Subramanian discloses an input recognizer embodied in a program storage device, said input recognizer configured to receive input from a user (Fig. 1B, configuration data inputted from a user are stored in a memory 118).

With respect to claim 22, Subramanian discloses that the reconfigurable logic core comprises a vector processor (Fig. 1B, DSP/uP 112).

With respect to claim 24, Subramanian discloses that wherein the digital portion comprises a reconfigurable processor core including the reconfigurable logic core and the plurality of general-purpose processor cores (Fig. 1B, the reconfigurable processor core including DSP/uP 112, processors 102a, 102b, 104).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 7, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al (US Pub 2002/0031166 A1) in view of Hartmann (US Patent No. 6,096,091).

With respect to claim 5, Subramanian discloses a memory positioned between the reconfigurable logic core and at least one of the one or more general-purpose processor cores (Fig. 1B, memory 106 positioned between processor 112 and processor 102a). Subramanian does not disclose that the memory is a FIFO memory. Hartmann discloses a FIFO buffer 120A positioned between the reconfigurable logic 110A and processor 150 (Fig. 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a FIFO buffer in Subramanian's system, as suggested Hartmann, to buffer data in a sequential order.

With respect to claims 7 and 17, Subramanian discloses a plurality of general-purpose processor cores (Fig. 1B, processors 102a, 102b, 104). Subramanian does not disclose a RISC processor. Hartmann discloses that the embedded processor 150 is RISC processor (col. 4, lines 47-54 and Fig. 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include RSIC processor in Subramanian's system, as suggested by

Hartmann, to reduce delay since RISC processors operate on a very limited number of instructions.

Allowable Subject Matter

8. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments filed June 16, 2006 have been fully considered but they are not persuasive.

Applicant argues in page 6 that instances of omitted periods set forth in the Office Action cannot be found. Applicant requests further explanation of this objection. According to the specification submitted on October 9, 2001, in the 3rd paragraph, in line 17, there was no period inserted to terminate the sentence and the paragraph, e.g., after "throughput of 802.11B transceivers". Similar omitted periods can be found throughout the specification as stated in the objection to the disclosure.

Applicant argues in page 6 that Subramanian does not disclose that the reconfigurable logic core coupled to receive a digitized RF signal from an ADC. Examiner respectfully disagrees. As clearly illustrated in Fig. 1B, the interface conversion/sector combining 116, including the ADC, coupled to the DSP/uP 112 via a bi-directional bus.

Applicant argues in page 6 that the modem processor 102 and codec processor 104 are not general-purpose processors. Examiner respectfully disagrees. General-purpose processors are processors for performing some purposes in general. Therefore, modem processor and codec

processor are processors for performing some functions in general. Further, claim 1 does not recite that general-purpose processors are not operation-specific or algorithm-specific processors.

Applicant argues in page 6 that Subramanian does not disclose that the device can handle a short-range wireless protocol, as recited in claim 2. Examiner respectfully disagrees. As clearly recited in claim 2, in lines 2-3, the limitation "includes one or more" limits the choice to one of the followings. Therefore, Examiner does not have to consider the short-range wireless protocol as argued by the Applicant.

Applicant argues in pages 6 and 7 that Subramanian does not disclose a router that routes packets to a cellular radio core and a short-range wireless transceiver core, as cited in dependent claim 8. Examiner respectfully disagrees. Subramanian discloses in Fig. 1B, configurable modem processor 102a routes data packets to interface conversion/sector combining 116 operable with cellular and 802.11 protocols. Further, applicant argues in page 7 that the claims 18-20 contain similar subject matter as in claims 8-10. Examiner respectfully disagrees. Claims 8-10 and 18-20 are different in scope, e.g., claim 18 does not recite routing packets to a cellular radio core and a short-range wireless transceiver core of the analog portion.

Applicant argues in page 7 that Subramanian does not disclose a vector processor as recited in claim 22. Examiner respectfully disagrees. The DSP/uP 112 as illustrated in Fig. 1B is the vector processor.

Applicant argues in pages 7 and 8 that Hartmann fails to teach that the buffer is positioned between reconfigurable logic core and the general-purpose processor core and there is no motivation to combine the two teachings. Examiner respectfully disagrees. First of all, Hartmann reference is only relied upon to show that the buffer is a FIFO buffer. Subramanian

taught the positioning. Secondly, since FIFO buffer is well known in the art for storing data to be processed according to their arrival. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a FIFO buffer in Subramanian's system, as suggested Hartmann, to buffer data in a sequential order for processing.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H. Ly whose telephone number is 571-272-3175. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

avl

CHI PHAM
SUPERVISORY PATENT EXAMINER